AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-22. (canceled)

23. (currently amended) An integrated circuit comprising:

a bus; and

a plurality of devices coupled to the bus in which individual devices include respective agents coupled to the bus to receive a clock signal having a rising edge and a falling edge, the agents to drive an arbitration signal onto the bus responsive to one of the rising or falling edge and to sample ~~and evaluate~~ the arbitration signal on the bus responsive to other of the falling or rising edge and to evaluate the arbitration prior to a subsequent cycle of the clock cycle to allow one agent to request and win arbitration of the bus in one clock cycle, the one agent winning arbitration to drive an address of a transaction responsive to one of the rising or falling edge of ~~a~~ the subsequent clock cycle and agents involved in coherency to sample and evaluate the address responsive to other of the falling or rising edge of the subsequent clock cycle and to respond with coherent response signals on the bus at a fixed number of clock cycle or cycles after the address to maintain order for coherency, but in which data driven onto the bus in response to the address need not be maintained at a fixed number of clock cycle or cycles after the address to allow data to be driven out of order on the bus.

24. (original) The integrated circuit of claim 23, wherein the plurality of agents are disposed in the individual devices to perform as distributed agents in a distributed arbitration scheme.

25. (original) The integrated circuit of claim 24, wherein the plurality of devices include a processor, cache memory, memory controller and input/output (I/O) interface, wherein

agents within the processor, cache memory, memory controller and I/O interface drive and sample signals on the bus responsive to rising or falling edges of the clock signal.

26. (previously presented) The integrated circuit of claim 25, wherein tags are placed and used to identify corresponding data to the address.

27. (original) The integrated circuit of claim 25, wherein the agents to drive the bus responsive to the rising edge and to sample responsive to the falling edge.

28. (original) The integrated circuit of claim 25, wherein the agents to drive the bus responsive to the falling edge and to sample responsive to the rising edge.

29. (currently amended) A method comprising:

driving arbitration signals on a bus of an integrated circuit having a plurality of devices coupled to the bus, in which individual devices include respective agents coupled to the bus to receive a clock signal having a rising edge and a falling edge, wherein the arbitration signals are driven onto the bus responsive to one of the rising or falling edge;

sampling ~~and evaluating~~ the arbitration signals responsive to other of the falling or rising edge;

evaluating the arbitration signal prior to a subsequent cycle of the clock cycle to allow one agent to request and win arbitration of the bus in one clock cycle;

driving an address of a transaction responsive to one of the rising or falling edge of ~~a~~ the subsequent clock cycle by the one agent winning arbitration of the bus;

sampling and evaluating the address responsive to other of the falling or rising edge of the subsequent clock cycle by agents involved in coherency;

responding with coherent response signals on the bus at a fixed number of clock cycle or cycles after the address by the agents involved in coherency to maintain order for coherency; and

driving data onto the bus in response to the address without maintaining fixed number of clock cycle or cycles after the address to allow data to be driven out of order on the bus.

30. (original) The method of claim 29, further comprising performing the driving and sampling on a plurality of agents that are distributed in a distributed arbitration scheme.

31. (previously presented) The method of claim 30, further comprising tagging address and data to identify corresponding address and data when data is driven out of order onto the bus.

32. (original) The method of claim 30, wherein the driving is responsive to the rising edge and sampling is responsive to the falling edge.

33. (original) The method of claim 30, wherein the driving is responsive to the falling edge and sampling is responsive to the rising edge.